Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BASE Q2**
2. **BASE Q3**
3. **EMITTER Q3**
4. **BASE Q1**
5. **SUBSTRATE**
6. **COLLECTOR Q5**
7. **COLLECTOR Q6**
8. **BASE Q6**
9. **EMITTER Q4**
10. **BASE Q4**
11. **BASE Q5**
12. **SUBSTRATE**
13. **COLLECTOR Q1**
14. **COLLECTOR Q2**

**.033”**

**.047”**

8229

**6 5 4 3 2**

**9 10 11 12 13**

**7**

**8**

**1**

**14**

**NOTE:** The substrate must be connected to the most negative point in the external

circuit to maintain isolation between transistors and to provide for normal

transistor action.

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 8229**

**APPROVED BY: DK DIE SIZE .033” X .047” DATE: 10/14/16**

**MFG: RCA THICKNESS .014” P/N: CA3102**

**DG 10.1.2**

#### Rev B, 7/1